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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/942,200

08/29/2001

Eugene P. Marsh

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08/22/2002

MUETING, RAASCH & GEBHARDT, P.A.

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EXAMINER

NGUYEN, JOSEPH H

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 08/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/942,200

Applicant(s)

MARSH, EUGENE P. 

Examiner

Joseph Nguyen

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 June 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 23-49 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 23-49 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 23-26 and 37-39 in Paper No. 5 is acknowledged. The traversal is on the ground(s) that figure 1 is generic to figures 2-5. This is found persuasive. Therefore, claims 23-39 are now rejoined and prosecuted together.

Claim Objections

Claims 27 and 31 are objected to because of the following informalities: in claim 27, the term "the first" in line 17 should be --"the first electrode"--. Also, in claim 31, the term "materials selected from materials selected" in line 2 should be --"materials selected"--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 23-24 and 26-48 are rejected under 35 U.S.C. 102(e) as being anticipated et al by Dornfest et al.

Regarding claim 23, Dornfest et al discloses on figure 2 a semiconductor device structure, the structure comprising a substrate assembly 31 including a surface; and a barrier layer 50 over at least portion of the surface, wherein the barrier layer 50 is formed of a platinum (X): ruthenium (1-X), where X is in the range of about 0.60 to 0.995 (col. 5, lines 15-28).

Regarding claim 24, Dornfest et al discloses on figure 2 X is in the range of about 0.90 to about 0.98 (col. 5, lines 25-27).

Regarding claim 26, Dornfest et al discloses on figure 2 the portion of the surface is a silicon-containing surface.

Regarding claim 27, Dornfest et al discloses on figure 2 a capacitor structure comprising a first electrode 38; a dielectric material 40 on at least a portion of the first electrode; and a second electrode 36 on the dielectric material, wherein at least one of the first and second electrode comprises a barrier layer 50 of platinum (X): ruthenium (1-X) alloy.

Regarding claim 28, Dornfest et al discloses on figure 2 X is in the range of about 0.60 to about 0.995 (col. 5, lines 15-28).

Regarding claim 29, Dornfest et al discloses on figure 2 X is in the range of about 0.90 to about 0.98 (col.5, lines 25-27).

Regarding claim 30, Dornfest et al discloses on figure 2 at least one of the first electrode and second electrode comprises the barrier layer 50 of platinum (X): ruthenium (1-X) alloy and one or more additional conductive layers 48, 46, 44.

Regarding claim 31, Dornfest et al discloses on figure 2 the one or more additional conductive layers 48, 46, 44 are formed from materials selected from the group of metals and metal alloys; metal and metal alloy oxide; metal nitrides and metal silicides.

Regarding claim 32, Dornfest et al discloses on figure 2 a memory cell structure comprising a substrate assembly including at least one active device 31; and a capacitor formed relative to the at least one active device, the capacitor comprising at least one electrode 38 including a barrier layer 50 formed of platinum (X): ruthenium (1-X) alloy.

Regarding claim 33, Dornfest et al discloses on figure 2 the capacitor includes a first electrode 38 formed relative to a silicon containing region of the at least one active device; a dielectric material 40 on at least a portion of the first electrode; and a second electrode 36 on the dielectric material, wherein the first electrode comprises the barrier layer 50 formed of platinum (X): ruthenium (1-X) alloy.

Regarding claim 34, Dornfest et al discloses on figure 2 the first electrode 38 comprising the barrier layer 50 formed of platinum (X): ruthenium alloy includes one or more additional conductive layers 48, 46, 44.

Regarding claim 35, Dornfest et al discloses on figure 2 X is in the range of about 0.60 to about 0.995 (col. 5, lines 15-28).

Regarding claim 36, Dornfest et al discloses on figure 2 X is in the range of about 0.90 to about 0.98

Regarding claim 37, Dornfest et al discloses on figure 2 an integrated circuit structure comprising a substrate assembly 31 including at least one active device 31; and an interconnect 38 formed relative to the at least one active device, the interconnect including a barrier layer 50 formed of platinum (X): ruthenium (1-X) alloy.

Regarding claim 38, Dornfest et al discloses on figure 2 X is in the range of about 0.60 to about 0.995 (col. 5, lines 15-28).

Regarding claim 39, Dornfest et al discloses on figure 2 X is in the range of about 0.90 to about 0.98.

Regarding claim 40, Dornfest et al discloses on figure 2 the barrier layer 50 comprises a chemical vapor deposited barrier layer (col. 9, lines 43-44).

Regarding claim 41, Dornfest et al discloses on figure 2 the at least a portion of the surface defines a small high aspect ratio opening.

Regarding claim 42, Dornfest et al discloses on figure 2 a thickness of the barrier layer 50 is in a range of about 10A to about 10,000A. (col. 6, lines 5- 7).

Regarding claim 43, Dornfest et al discloses on figure 2 the thickness of the barrier layer is in a range of about 100A to about 500A (col. 6, lines 5-7).

Regarding claim 44, Dornfest et al discloses on figure 2 the substrate assembly 31 comprises at least one active device.

Regarding claim 45, Dornfest et al discloses on figure 2 the barrier layer 50 comprises a chemical vapor deposited barrier layer (col. 9, lines 43-44).

Regarding claim 46, Dornfest et al discloses on figure 2 the substrate assembly comprises a small high aspect ratio opening, and further wherein the interconnect is formed in the small high aspect ratio opening relative to the at least one active device.

Regarding claim 47, Dornfest et al discloses on figure 2 a thickness of the barrier layer 50 is in a range of about 10A to about 10,000A.

Regarding claim 48, Dornfest et al discloses on figure 2 the thickness of the barrier layer is in a range of about 100A to about 500A.

Claims 23, 26, 27, 32, 37, 40, 41, 44 and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Wolters et al.

Regarding claims 23, 26, 27, 32, 37, 40, 41, 44 and 45, Wolters et al discloses on figure 6 all the structures set forth in claimed invention.

Claims 23, 26, 27, 32, 37, are rejected under 35 U.S.C. 102(e) as being anticipated by Kawakubo et al.

Regarding claims 23, 26, 27, 32 and 37, Kawakubo et al discloses on figure 5E all the structures set forth in claimed invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 25 and 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dornfest et al or Kawakubo et al as applied to claims 23 and 39 above.

Regarding claims 25 and 49, Dornfest et al or Kawakubo et al discloses substantially all the structure set forth in the claimed invention except X being about 0.95. However, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify Dornfest et al or Kawakubo et al by having X being about 0.95 for the purpose of improving the performance of the semiconductor device, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 5892254 to Park et al discloses an integrated circuit capacitor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN

August 16, 2002

A handwritten signature in black ink, appearing to read 'Eddie Lee', is positioned above the printed name.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800